IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 4, Issue 5, May 2016

Design and Analysis of Phase Locked Loop Based Frequency Synthesizer Using Source Coupled VCO

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Abstract: The CMOS PLL based Frequency Synthesizer is a vital role in Receiver front end Sub component. In general, the PLL contains PFD, Charge pump, Loop Filter, VCO and Frequency Divider, Voltage controlled oscillator (VCO) is a critical building block in PLL which decides the power consumed by the PLL and area occupied by the PLL. Here the Source Coupled VCO is proposed with adaptive voltage level technique to reduce the power consumption, then design of PLL and Clock recovery circuit by using different types of VCO and results are compared between them. It is designed in Tanner tool.

Keywords: Source Coupled VCO, PFD, PLL, CSVCO, Tanner tool, Frequency Divider and Charge Pump.

I. INTRODUCTION

A PLL is a feedback system that compares the output frequency/phase with the input frequency/phase. Phase-locked loops can be making used for frequency synthesizing, carrier synchronization, carrier recovery, frequency division, frequency multiplication and frequency Demodulation. A VCO is the compassion of the PLL and can be designed either by LC or RC. A LC VCOs have higher phase noise performance compared with ring VCO'S. Nevertheless, the LC VCO has a small tuning range for large layout area and probably has higher power. The ring oscillators do not have the problem of the on-chip inductors vital for the LC oscillators. Hence, the chip area is reduced. The phase noise performance of ring oscillators is much poorer in general. In addition, by the side of high oscillation frequencies, the power consumption of the ring oscillators possibly will not be low which a key requirement for battery-operated devices is. To resolve these complications, we put effort on single stage source coupled VCO exclusive of using an LC tank circuit.

Current work is done with major intention of reduced power consumption in design of VCO with different reduction techniques. The main part of this PLL is the SCVCO, which has been designed to get superior phase noise.

A. SYSTEM OVERVIEW

The Phase-locked loops (PLLs) generate timely on-chip clocks for different applications such as clock and data recovery, microprocessor clock generation and frequency synthesizer. A PLL is a closed-loop feedback system set predetermined phase correlation between its output clock phase and the phase of a reference clock. A PLL follow the phase changes that are within the bandwidth of the PLL. A PLL is a negative feedback control system circuit. As the name means, the intention of a PLL is to generate a signal during which the phase is same compared to the phase of a reference signal. This is prepared subsequent to many iterations of comparing the reference and feedback signals. Overall target of the PLL is to match the phase of the reference and feedback signals during the lock mode during which PLL output is constant. Afterwards, the PLL prolongs to compare the two signals. A basic form of a PLL consists of four main blocks:

1. Phase Frequency Detector (PFD)
2. Charge pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
5. Frequency divider (or) Programmable Counter (÷N)

B. PLL ARCHITECTURE

To synchronize the frequency, different types of PLLs are being used in the application of wireless communication. PLLs are contains of PFD, CP, LPF, SCVCO and frequency divider. This is shown in Fig. 1. In addition to SCVCO and PFD compares feedback signal through input signal and generates the error signal.

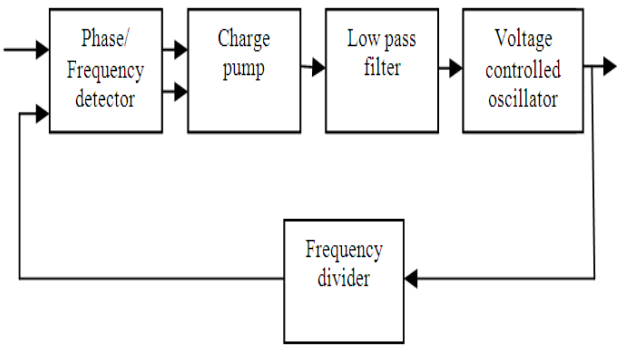

Fig.1.The block diagram of PLL

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A charge pump circuit is next to the LPF is used to minimize the conflicts at the input of SCVCO and to get a sharper and flat signal at the SCVCO output. To shape a phase-locked loop (PLL) and the phase error output of PFD is provided to a charge pump. Then the low pass filter mixes the signal to acquire a sharper and smooth signal. Therefore, the conflicts at the input of SCVCO get diminished.

II. CONVENTIONAL METHODS

The conventional methods enables the study of different types of VCO and certain parameter like tuning range, phase noise, oscillation frequency. The conventional method includes the design of ring oscillator and current starved VCO.

2.1 Ring oscillator.

A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of π=N, where N is the number of delay stages. The remaining phase shift is provided by a dc inversion. This means that for an oscillator with single-ended delay stages, an odd number of stages are necessary for the dc inversion.

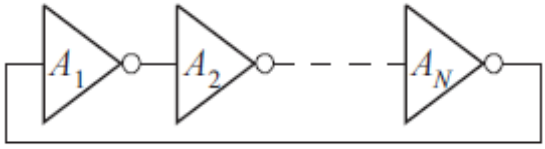

Fig 2.1: The ring oscillator.

2.2 CURRENT STARVED VCO (CSVCO).

The current-starved VCO is similar to the ring oscillator. MOSFETs M2 and M3 operate as an inverter, while MOSFETs Ml and M4 operate as current sources. The current sources, Ml and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for current. The MOSFETs M5 and M6 drain currents are the same and are set by the input control voltage. The currents in M5 and M6 are mirrored in each inverter/current source stage.

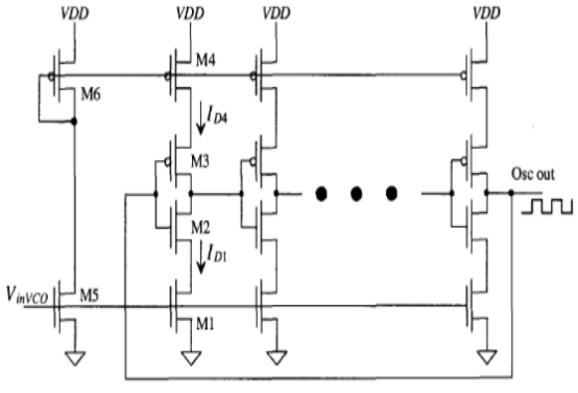

Fig 2.2: The block diagram of CSVCO.

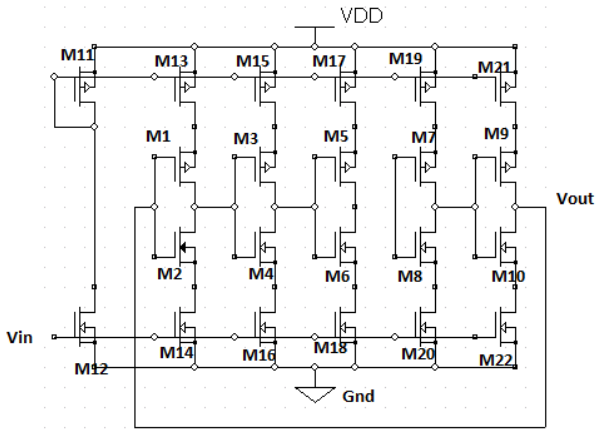

Fig 2.3: Schematic of 5 stage CSVCO.

III. PROPOSED METHOD

The proposed method includes the design of single stage source coupled VCO with adaptive voltage technique.

3.1 SOURCE COUPLED VCO (SCVCO).

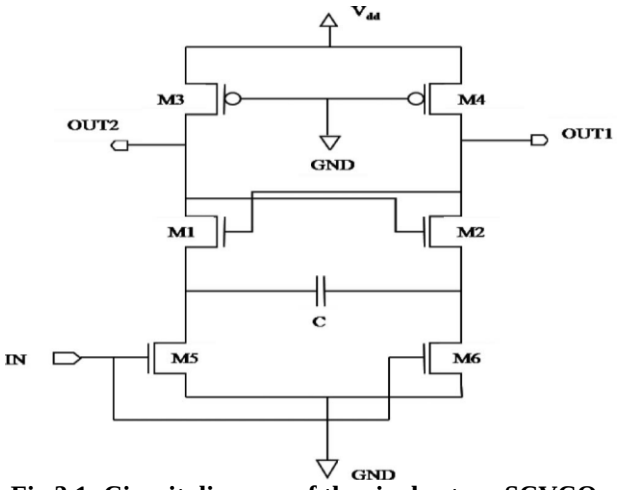

Fig 3.1: Circuit diagram of the single-stage SCVCO.

In the above Fig 3.1, the MOSFETs M1 and M2 act as switches, MOSFETs M3 and M4 pulled the output. The MOSFETs M5 and M6 behave as a constant current source. MOSFETs M2 is on and M1 is off, because the voltage of terminal 2 outputs (out2) is less than the terminal 1 output (out1), so the current in M2 is 2Id and capacitor will be changed by current Id, because M6 has Id sinking current.

In this Adaptive Voltage Level technique the power consumption can be reduced. In order to reduce the power consumption an additional control circuit which can be used at the upper end of the circuit to bring down the supply voltage value .It would reduce power leakage on each transistor known as Adaptive Voltage Level at Supply (AVLS) technique. Likewise we also have another control circuit which can be use at the lower end of the circuit to lift the ground potential. It would also reduce the power leakage known as Adaptive Voltage Level at Ground (AVLG) technique. The complete effect of these techniques on the power consumption can be described as follows.

DOI 10.17148/IJIREEICE.2016.4570

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AVLG technique:

In Adaptive Voltage Level at Ground (AVLG) technique the additional control circuit consists of combination of 1-NMOS and 2-PMOS transistors which are connected in parallel. Additionally an input clock is applied at the input terminal of the NMOS transistor in the control circuit and the rest of the PMOS transistors in the control circuit are connected to the ground terminal. It would lift the ground potential of the circuit to reduce the power consumption of the SCVCO design. Depending upon the input the output also varied and the usage of clock is to prevent any defect in circuit function during power consumption.

AVLS technique:

In Adaptive Voltage Level at Supply (AVLS) technique the additional control circuit is made up of combination of 1 PMOS and 2 NMOS transistor connected in parallel. At which an input clock is applied at the input terminal of the PMOS transistor and the rest of the NMOS transistor is connected to the drain terminal. This AVLS control circuit is placed at voltage supply source terminal in which supply is given through this control circuit. This control circuit at the upper end would bring down the supply voltage given to the whole circuit in order to reduce the power consumption of the SCVCO design. When the input is varied corresponding output will be produced. It would reduce the leakage power by reducing the gate to source voltage and gate to drain voltage. This design would be responsible for very low power consumption.

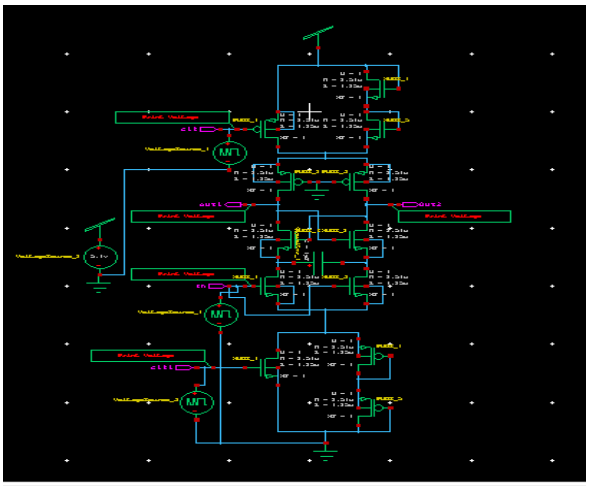

Fig 3.2: The SCVCO with AVL technique.

IV. RESULTS

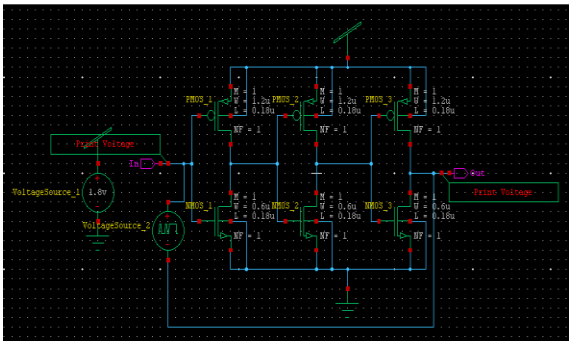

Fig 4.1: 3 stage Ring VCO.

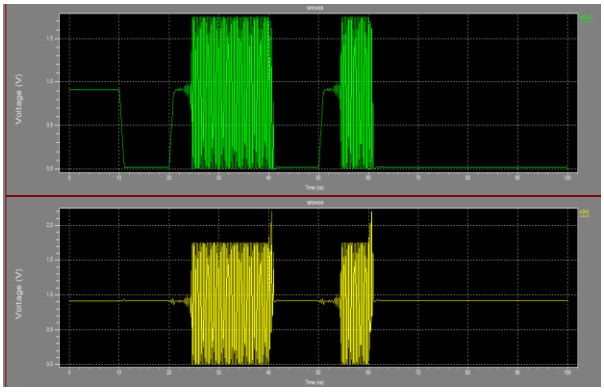

Fig 4.2: The output waveform of 3 stage Ring VCO

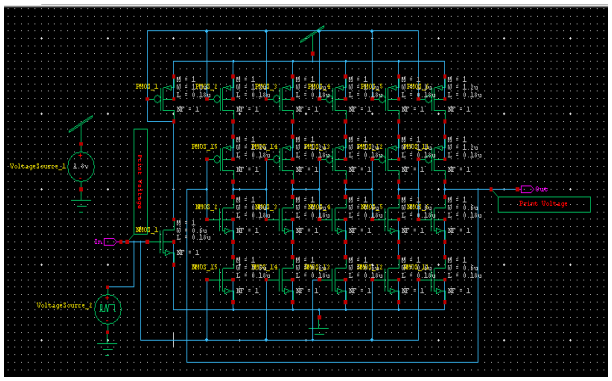

Fig 4.3: The schematic of 5 stage CSVCO.

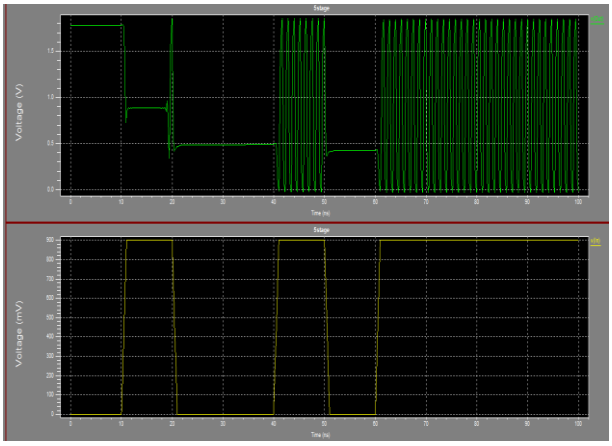

Fig 4.4: The output of 5 stage CSVCO

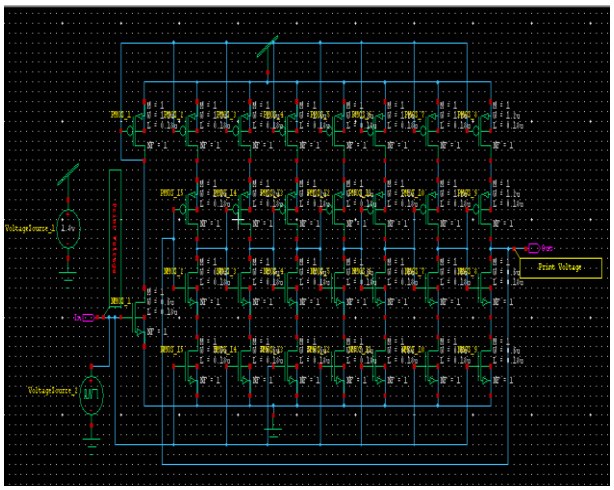

Fig 4.5: the schematic of 7 stage CSVCO

DOI 10.17148/IJIREEICE.2016.4570

IJIREEICE

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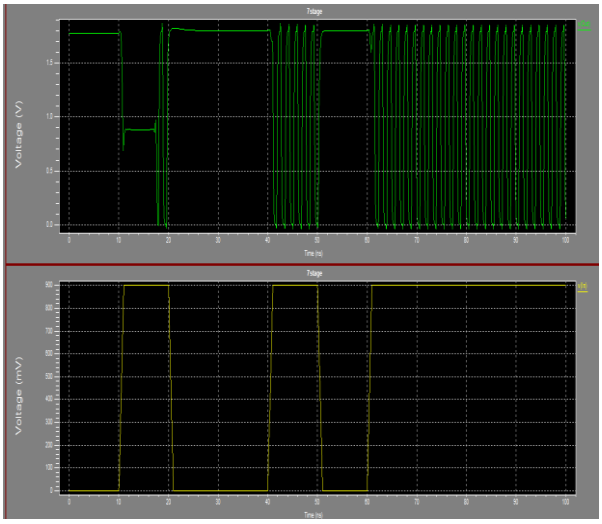

Fig 4.6: The output of 7 stage CSVCO

The Fig 4.7 shows the output of SCVCO, it has two output both output are 180 out of phase with each other.

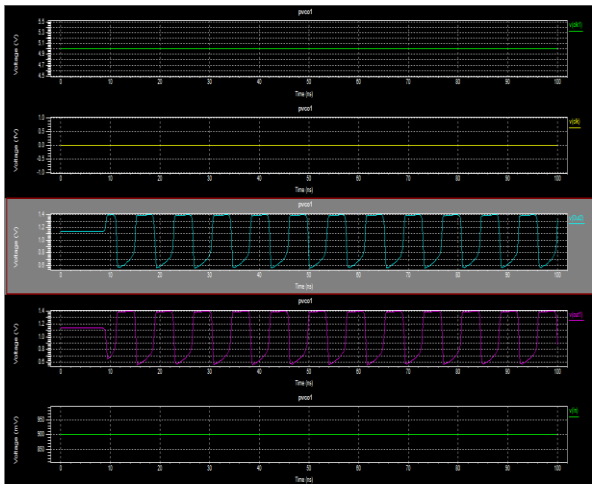

Fig 4.7: The output waveform of SCVCO

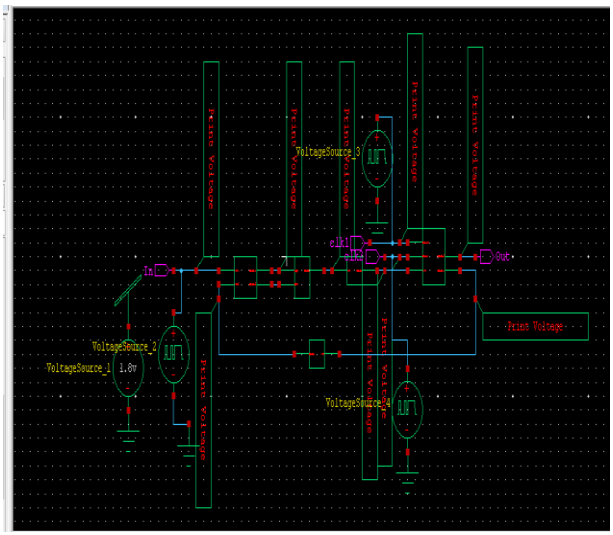

Fig 4.8: The schematic of PLL

The Fig 4.9 shows simulation result of PLL are carried out by using Tanner tool, here T- Spice circuit simulator are used.

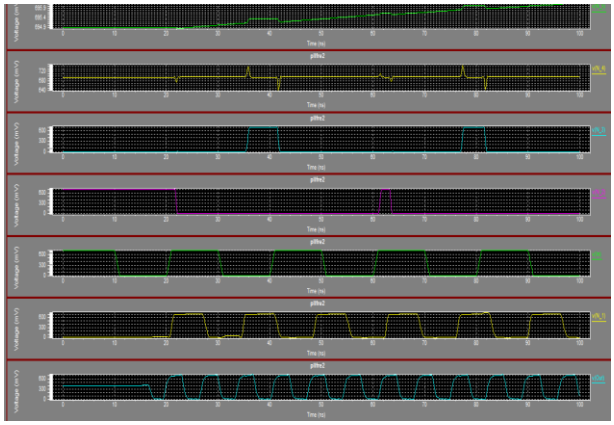

Fig 4.9: The output waveform of PLL

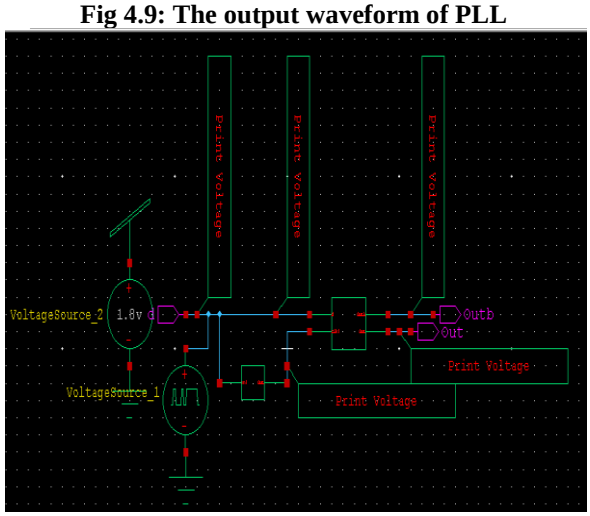

Fig 4.10: The schematic of clock recovery circuit.

The Fig 4.11 shows the output waveform of clock recovery circuit, it can be designed by using D flip flop and PLL. The data input to the D flip flop is applied as input to PLL then output of PLL is applied as clock input to D flip flop.

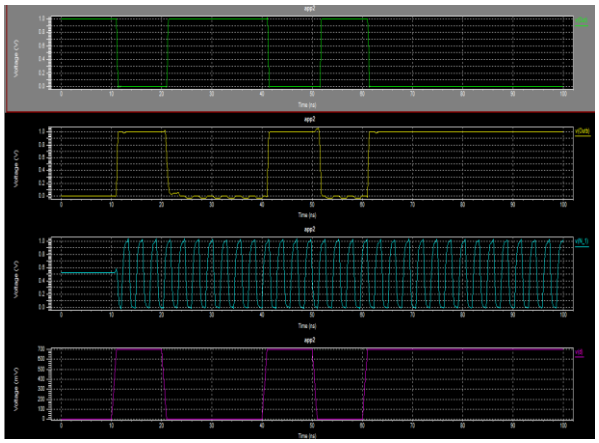

Fig 4.11: The output waveform of clock recovery circuit.

Table 4.1: Comparison table

Parameter	Ring VCO	5 stage CSVCO	7 stage CSVCO	SCVCO
Power (mW)	21.3	20.23	21	19.33

DOI 10.17148/IJIREEICE.2016.4570

The Table 4.1 shows power consumed by different types of VCO

Table 4.2: Comparison table

Parameter	Ring VCO	5 stage CSVCO	7 stage CSVCO	SCVCO
Power (mW)	51.7	56.28	56.36	30.22

The Table 4.2 shows power consumed by PLL with different types of VCO.

Table 4.3: Measurement result

Parameter	Ring VCO	5 stage CSVCO	7 stage CSVCO	SCVCO
Power (mW)	54.3	58.1	58.6	18.45

The Table 4.3 shows power consumed by clock recovery circuit with different types of VCO.

V. CONCLUSION

Modern wireless communication systems require phase locked loop (PLL) mainly on synchronization clock synthesis, skew and jitter reduction. Here PLL based frequency synthesizer was designed using different types of VCO, then result are compared depending on the power consumed by those VCO's. Hence we can conclude while increasing the number of stages for getting the higher frequency the power dissipation and size of oscillator was going to increase.

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